REMARKS

Claims 1-8, and 11-22 were pending in the present application. Claims 2, 16, 20, and 21 have been cancelled. Claims 1, 3, 5, 7, 11, 17-19, and 22 have been amended. Claims 1, 3-8, and 11-15, 17-19, and 22 accordingly remain pending in the application.

Claims 16 and 17 are objected to for failing to comply with C.F.R. 1.75(c) as being of improper antecedent form. Applicant has cancelled claim 16 and corrected the dependency of claim 17.

Claims 1, 2, 13, 18 and 20-22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Li (U.S. Patent No. 6,760,577) (hereinafter "Li") in view of Healey et al.(U.S. Patent No. 4,434,407) (hereinafter "Healey"). Although Applicant respectfully traverses at least portions of this rejection, Applicant has amended the claims to expedite allowance.

Claims 3-5, 7, 8, 11, 12, 16, and 19 stood rejected under U.S.C. 103(a) as being unpatentable over Li in view of Healey, and in further view of Wu, et al (U.S. Patent No. 6,968,167) (hereinafter "Wu"). Applicant respectfully traverses this rejection.

Claim 6 stood rejected under U.S.C. 103(a) as being unpatentable over Li in view of Healey, in view of Wu, and in further view of Huscroft et al (U.S. Patent No. 5,512,860) (hereinafter "Huscroft"). Applicant respectfully traverses this rejection.

Claims 14 and 15 stood rejected under U.S.C. 103(a) as being unpatentable over Li in view of Healey, and in further view of Liu (U.S. Patent No. 7,184,737) (hereinafter "Liu"). Applicant respectfully traverses this rejection.

Applicant's claim 1, as amended, recites a receiver circuit comprising in pertinent part,

"an oscillator circuit including ***an*** oscillator configured to generate an oscillator signal, wherein the oscillator signal is divided by a first amount to generate a calibration tone and by a second amount to generate a phase locked loop (PLL) reference signal;

...

a second switch coupled to selectively provide the PLL reference signal to the phase locked loop circuit during the calibration mode of operation and a different reference signal to the phase locked loop circuit during a normal mode of operation."

Applicant submits **none** of the cited references teach or suggest the combination of features recited in Applicant's claim 1. Specifically, in the rejection of claims 5, 7, 20, and 21, the Examiner asserts Li teaches the oscillator circuit including dividers (e.g., N1 and N2) that divide the reference signal by a first amount and second amount to generate the PLL reference signal and calibration tone. Applicant respectfully disagrees.

Li actually discloses in FIG. 3 the reference oscillator REF, providing the reference signal to the PLL1 block of the first fractional PLL. The divide N1 block referred to by the Examiner is actually dividing the output of the PLL Main VCO to obtain the reference oscillator signal frequency, and not dividing the Ref oscillator signal to obtain the PLL reference signal as suggested by the Examiner. The same is true for the calibration tone. The divider N2 of Li is dividing the pilot tone VCO signal obtain the reference oscillator signal frequency, and not dividing the Ref oscillator signal to obtain the calibration tone as suggested by the Examiner. Wu merely teaches dividing an oscillator signal to generate a single PLL reference signal.

In addition, none of the references teach or suggest "a second switch coupled to selectively provide the PLL reference signal to the phase locked loop circuit during the calibration mode of operation, **and** to provide a different reference signal to the phase locked loop circuit during a normal mode of operation," as recited in Applicant's claim 1.

Accordingly Applicant submits claim 1, along with its dependent claims, patentably distinguishes over the cited references for the reasons given above.

Applicant's claims 18 and 22 recite features that are similar to the features recited in claim 1. Thus, for at least the reasons given above, Applicant submits claims 18 and 22, along with their respective dependent claims patentably distinguish over the cited references.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5797-00100/SJC.

Respectfully submitted,

/ Stephen J. Curran /
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